









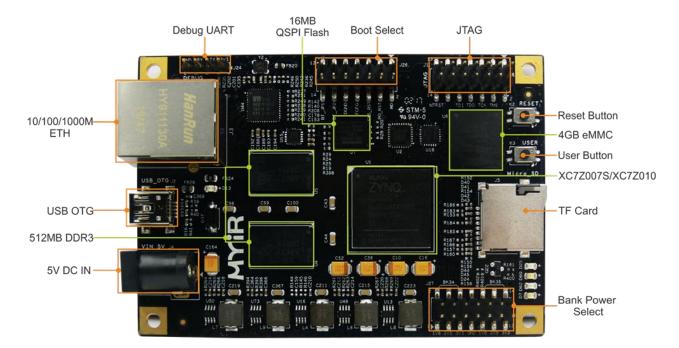
- ✓ 667MHz Xilinx XC7Z010 ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic
- ✓ 512MB DDR3 SDRAM (2 x 256MB, 32-bit), 4GB eMMC Flash, 16MB QSPI Flash
- ✓ USB2.0 OTG, 10/100/1000M Ethernet, TF, Debug UART, JTAG ···
- ✓ One 120 Position Connector Socket for Expansion interface
- ✓ Ready-to-Run Linux Single Board Computer
- ✓ Optional Camera and LCD Modules, IO Extension Cape



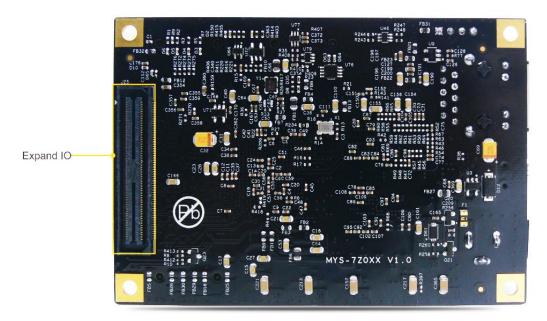


The **Z-turn Lite** is an ultra-cost-effective lite version of MYIR's **Z-turn board**. It is built around 766MHz Xilinx **Zynq-7010** SoC which is among the Zynq Z-7000 family with a dual-core **ARM Cortex-A9** processor and integrated Artix-7 Field Programmable Gate Array (**FPGA**) logic. It is a minimal and compact system of **Xilinx Z-7010** SoC and provides numerous pending configuration of PL resources. It is an excellent reference design and evaluation board for development based on **Xilinx Zynq-7000** series SoCs.

The **Z-turn Lite** takes full features of the **Z-7010** all programmable SoC. It is equipped with **512MB DDR3**, **4GB eMMC Flash**, **16MB QSPI Flash** and a set of peripherals including **Micro USB OTG**, **10/100/1000Mbps Ethernet**, **TF**, **JTAG**, **Debug UART**, etc. Additionally, there is one **120 position connector socket** on the rear of the board to bring out as many as IO signals for user extensions.



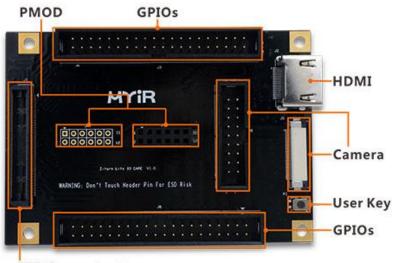
Z-turn Lite (Top-view)



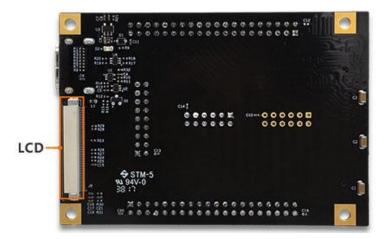
Z-turn Lite (Bottom-view)



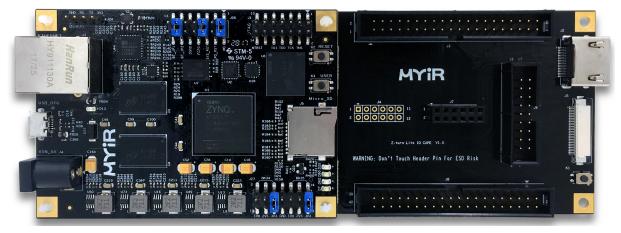
The **Z-turn Lite** is capable of running Linux operating system and provided with **Linux 4.14.0** SDK, the kernel and many drivers are in source code. The **Z-turn Lite Kit** is delivered with complete accessories including one micro-USB cable, one Ethernet cable, one 4GB TF card, one USB-to-UART cable, one 5V power adapter and product disk which enables you to start the development quickly when getting the board out-of-the-box. MYIR also offers optional camera and LCD modules as well as an I/O expansion board **Z-turn Lite IO Cape** for Z-turn Lite which provides many peripheral signals and interfaces including HDMI, GPIO, LCD, Camera and Pmod interfaces.



BTB Connector to Z-turn Lite



Z-turn Lite IO Cape



Z-turn Lite connected with Z-turn Lite IO Cape



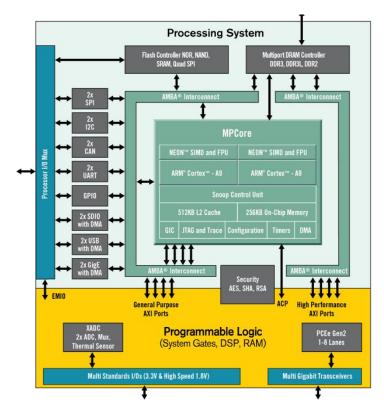


Hardware Specification

The **Zynq®-7000 All Programmable SoC** (AP SoC) family integrates the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device. Consisting of dual-core Zynq-7000 devices, the Zynq-7000 family is the best price to performance-per-watt, fully scalable SoC platform for your unique application requirements.

Zynq-7000

Zynq-7000 devices are equipped with dual-core ARM Cortex-A9 processors integrated with 28nm Artix-7 or Kintex®-7 based programmable logic for excellent performance-per-watt and maximum design flexibility. With up to 6.6M logic cells and offered with transceivers ranging from 6.25Gb/s to 12.5Gb/s, Zynq-7000 devices enable highly differentiated designs for a wide range of embedded applications including multi-camera drivers assistance systems and 4K2K Ultra-HDTV.



Zyng Z-7000 SoC Device Block Diagram





Zynq®-7000 All Programmable SoC Family Mid-Range Devices Z-7035 Z-7045 Part Number | XC720075 XC720125 XC720145 XC72010 XC72015 XC72016 | XC72015 XC72016 | XC72016 | XC72016 | XC72016 | XC72017 | X XC7Z030 XC7Z035 Z035 XC7Z045 Dual-Core ARM XC7Z100 Cortex-A9 MPCore Up to 1GHz⁽¹⁾ Engine and Single/Double Precision Floating Point Unit per processor L1 Cache 32KB Instruction, 32KB Data per processo L2 Cache 512KB On-Chip Memory External Memory Support^{[2} External Static Memory Support^{[2} DDR3, DDR3L, DDR2, LPDDR2 2x Quad-SPI, NAND, NOR 8 (4 dedicated to PL) DMA Channel 2x UART, 2x CAN 2.08, 2x I2C, 2x SPI, 4x 32b GPIO 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot 2x AXI 32b Master, 2x AXI 32b Slave Peripherals Peripherals w/ built-in DMA⁽²⁾ Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) 4x AXI 64b/32b Me AXI 64b ACP Artix-Artix-28K Kintex®-Kintex-**Logic Cells** 17,600 35,200 2.1Mb (60) Look-Up Tables (LUTs) 14,400 34,400 40,600 46,200 53,200 78,600 171,900 343,800 218,600 277,400 554,800 Flip-Flops Total Block RAM (# 36Kb Blocks) 68,800 2.5Mb (72) 81,200 3.8Mb (107) 92,400 3.3Mb (95) 106,400 4.9Mb (140) 157,200 9.3Mb (265) 437,200 19.1Mb (545) 17.6Mb (500) 1.8Mb 160 2,020 DSP Slice: 120 170 220 400 900 Gen2 x8 PCI Express Gen2 x4 Gen2 x8 Gen2 x8 Analog Mixed Signal (AMS) / XADC⁽²⁾ Security⁽³⁾ Commercial Speed Grades Extended Secure Programmable Logic Config -1, -2, -2L

Zynq Z-7000 SoC Device Table

The Z-turn Lite is based on the Xilinx Zynq-7010 SoC and the hardware specification is listed in following table 1-1:

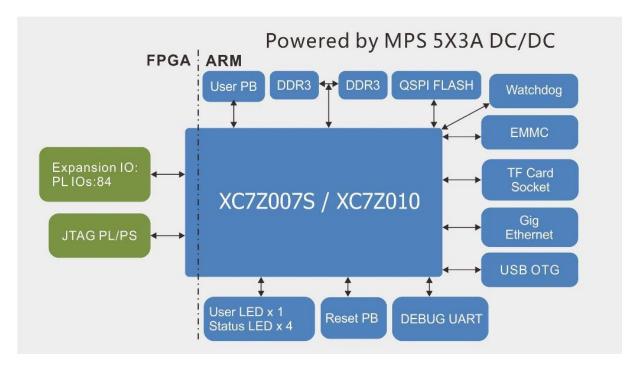
Item	Features		
	Xilinx XC7Z010-1CLG400C (Zynq-7010)		
	- 667MHz dual ARM® Cortex™-A9 MPCore processor		
	- Integrated Artix-7 class FPGA subsystem		
SoC	with 28K logic cells, 17,600 LUTs, 80 DSP slices (for XC7Z010)		
	- NEON™ & Single / Double Precision Floating Point for each processor		
	- Supports a Variety of Static and Dynamic Memory Interfaces		
Memory	512MB DDR3 SDRAM (2 x 256MB, 32-bit)		
Storage	4GB eMMC Flash		
	16MB QSPI Flash		
	TF card interface		
Communications	1 x 10/100/1000M Ethernet		
	1 x Micro USB2.0 OTG		
	1 x 2.54mm pitch 14-pin JTAG interface		
Input and Output	1 x 0.5mm pitch 120 Position Connector Socket for Expansion interface		
	1 x 2.54mm pitch 4-pin Debug UART interface		
	2 x Buttons (1x Reset, 1 x User)		
	5 x LEDs		
	- 1 x User LED		
Others	- 1 x FPGA configuration indicator		
	- 1 x FPGA initialization indicator		
	- 1 x Power indicator		
	- 1 x USB overcurrent indicator		
Dimensions	91mm x 63mm (10-layer PCB design)		
Power supply	DC 5V/2A		
Temp.	0~70 Celsius		
Power consumption	8W		
	7 to the Hand one Constitution		

Z-turn Lite Hardware Specification

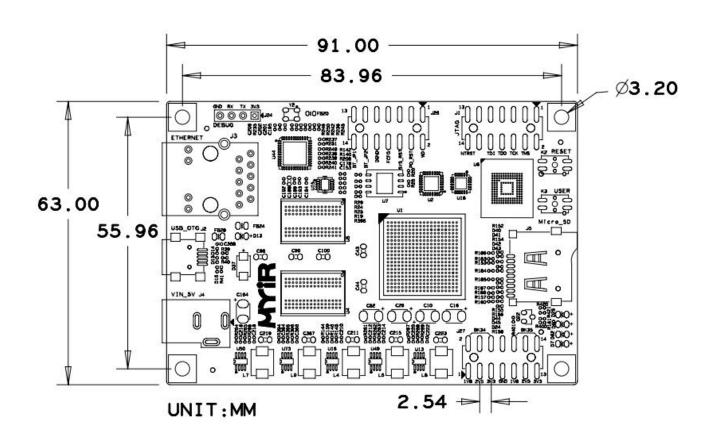
^{1. 1} GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. See <u>IDS180</u>, Zymp-7000 All Programmable SoC Overview for details. 2.2-7007s and 2-7010 in CL0225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to <u>UG585</u>, Zymp-7000 All Programmable SoC Technical Reference Manual for more details. 3. Security block is shared by the Processing System and the Programmable Logic.







Z-turn Lite Function Block Diagram



Z-turn Lite Dimension Chart





Software Features

Item	Features	Description	Remark
Cross compiler gcc 6.2.1		gcc version 6.2.1 (Linaro GCC Snapshot 6.2-2016.11)	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream and u-boot	Source code provided
Linux Kernel	Linux 4.14.0	Customized kernel for Z-turn Lite Board	Source code provided
Drivers	USB OTG	USB OTG driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	HDMI	HDMI driver	Source code provided
	LCD	LCD touch screen driver	Source code provided
File System	Ramdisk	Ramdisk image system	
	Rootfs	Rootfs image system (with QT5.11.3)	Source code provided

Software Features of Z-turn Lite



Order Information

Item	Part No.	Packing List
		✓ One Z-turn Lite (with XC7Z010-1CLG400C SoC)
Z-turn Lite	MYS-7Z010-L-C-S	✓ One Quick Start Guide
		✓ One 16GB TF card
Z-turn Lite Kit		✓ One Z-turn Lite (MYS-7Z010-L-C-S)
		✓ One Quick Start Guide
	MYS-7Z010-L-C	✓ One 1.5m cross Ethernet cable
		✓ One 1.2m Micro USB2.0 cable
		✓ One USB-to-UART cable
		✓ One 16GB TF card
		✓ One 5V/2A Power adapter
MY-CAPE002		Z-turn Lite IO Cape
MY-TFT070CV2		MY-TFT070CV2 7-inch LCD Module
		(Support through Z-turn Lite IO Cape,
		with capacitive touch screen)
MY-CAM002U		USB Camera Module



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