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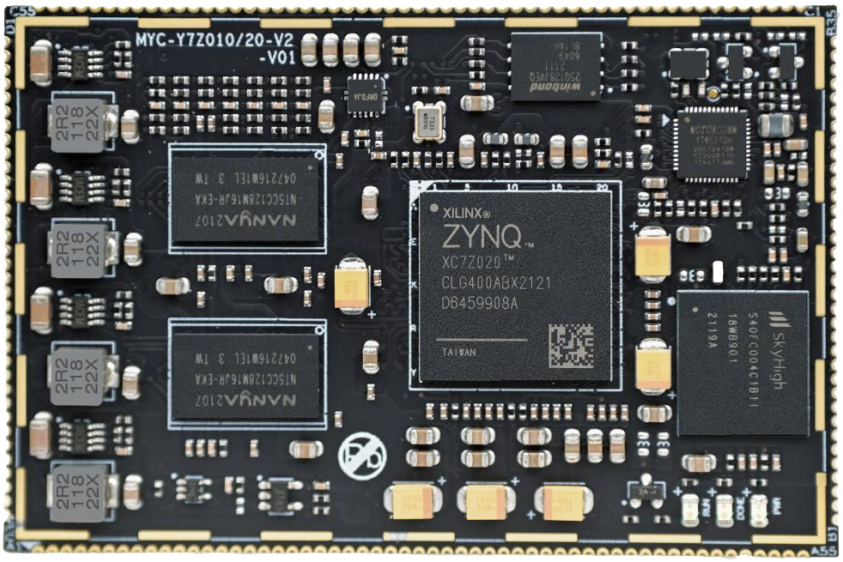
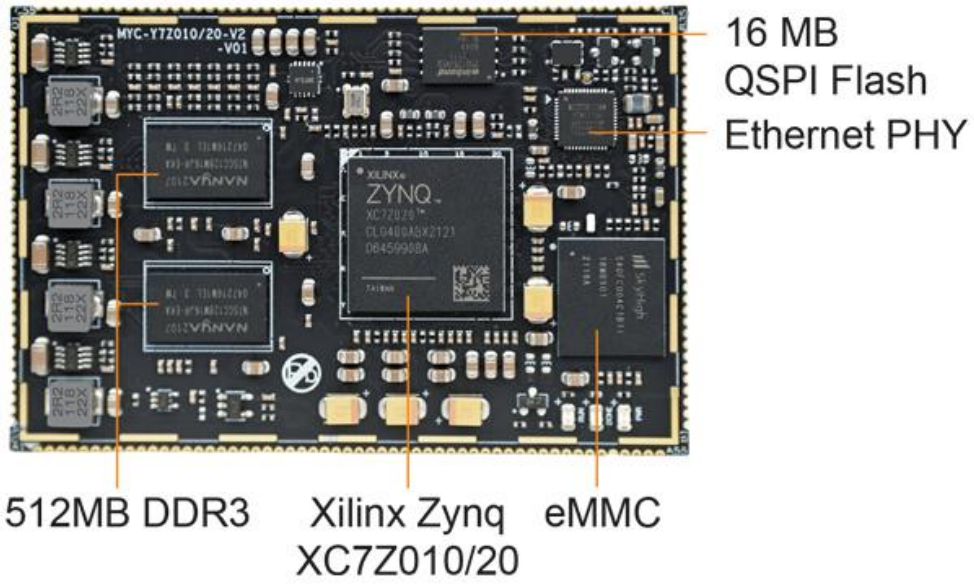
MYC-Y7Z010/20-V2 CPU Module

Overview



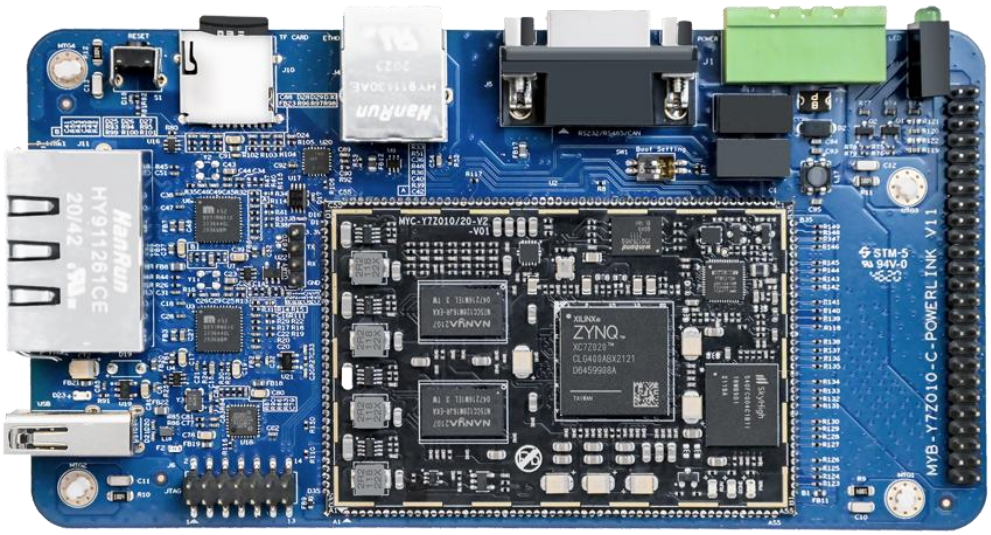
- ✓ *667MHz Xilinx XC7Z010/20 ARM Cortex-A9 Processor with Xilinx 7-series FPGA logic*
- ✓ *512MB DDR3 SDRAM (2 x 256MB, 32-bit), 4GB eMMC, 16MB QSPI Flash*
- ✓ *On-board Gigabit Ethernet PHY*
- ✓ *1.27mm pitch 180-pin Stamp Hole Expansion Interface*
- ✓ *Ready-to-Run Linux 4.14*
- ✓ *Supports -40 to +85 Celsius Extended Temperature Operation for Industrial Applications*

The **MYC-Y7Z010/20-V2 CPU Module** is an industrial-grade System-on-Module (SoM) based on Xilinx **Zynq-7000** family SoC available for either the XC7Z020 or XC7Z010 version. It has integrated the **Zynq-7020** or **Zynq-7010** device, 512MB DDR3 SDRAM, 4GB eMMC, 16MB quad SPI Flash, a Gigabit Ethernet PHY and external watchdog on board and provides 1.27mm 180-pin stamp-hole (Castellated-Hole) expansion interface to allow a large number of I/O signals for ARM peripherals and FPGA I/Os to be extended to your base board. The module is ready to run Linux and supports wide working temperature ranging from -40 to +85 Celsius which is ideal for industrial embedded applications.



MYC- Y7Z010/20-V2 CPU Module

MYIR provides a development board **MYD-Y7Z010/20-V2** for evaluating the **MYC-Y7Z010/20-V2 CPU Module**, which employs the MYC-Y7Z010/20-V2 as the controller board by populating the CPU Module on its base board through 1.27mm pitch 180-pin stamp-hole (Castellated-Hole) interface. The base board has extended a rich set of peripheral interfaces including serial ports, USB Host port, three Gigabit Ethernet ports, CAN, TF card slot, JTAG, etc. One 2.54mm pitch 2 x 25-pin expansion header is on the base board to let more GPIOs available for further extension.



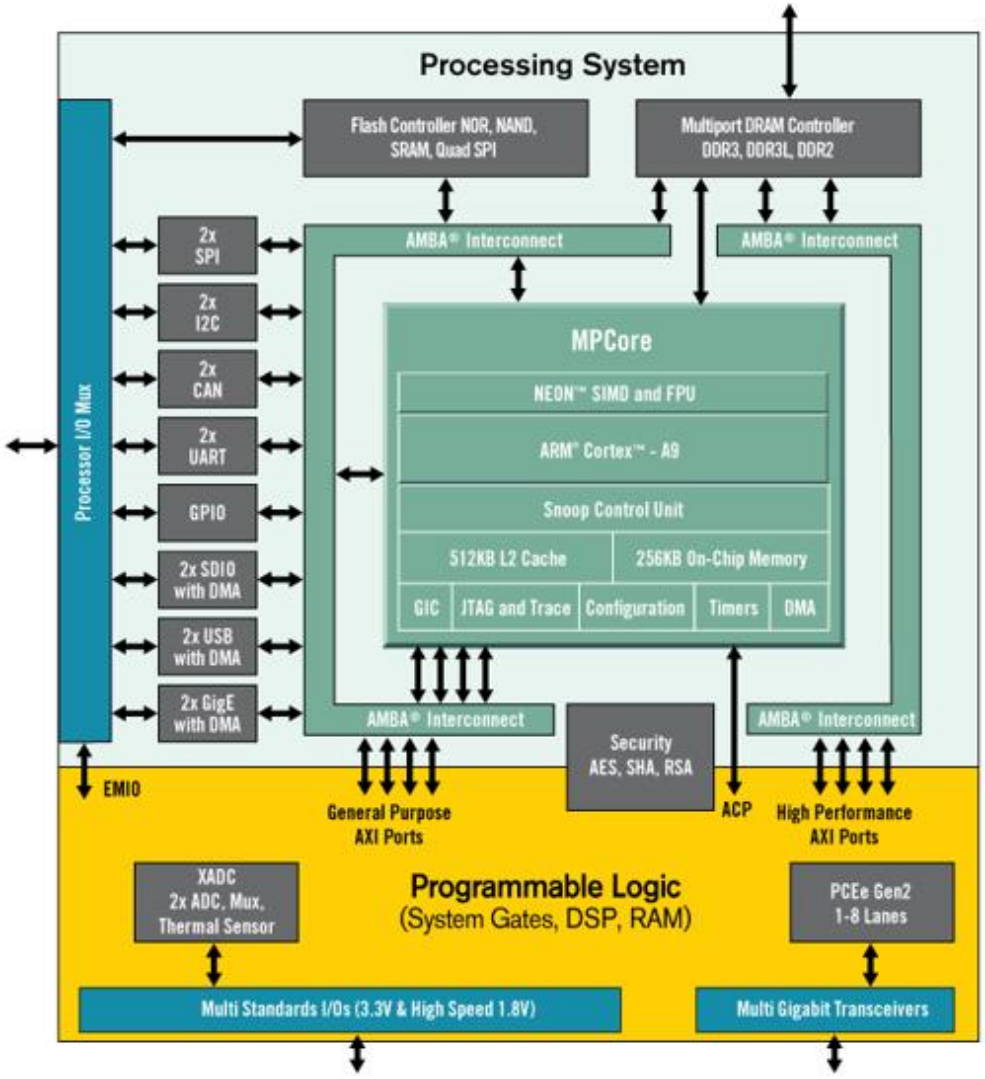
MYD-Y7Z010/20-V2 Development Board

Hardware Specification

The Zynq®-7000 All Programmable SoC (AP SoC) family integrates the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device. Consisting of single-core Zynq-7000S and dual-core Zynq-7000 devices, the Zynq-7000 family is the best price to performance-per-watt, fully scalable SoC platform for your unique application requirements.

Zynq-7000S

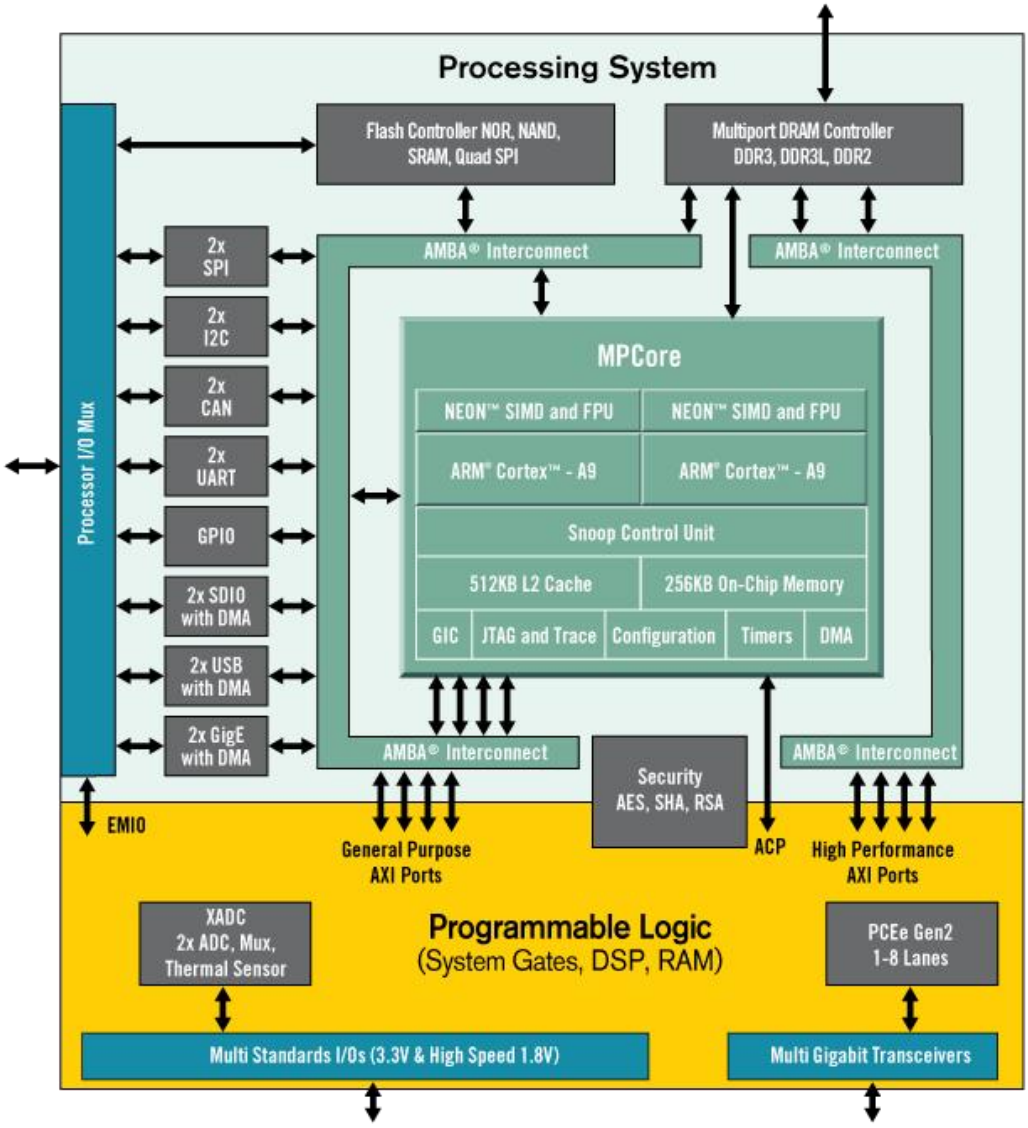
Zynq-7000S devices feature a single-core ARM Cortex™-A9 processor mated with 28nm Artix®-7 based programmable logic, representing the lowest cost entry point to the scalable Zynq-7000 platform. It includes Zynq Z-7007S, Z-7012S and Z-7014S which target smaller embedded designs. Available with 6.25Gb/s transceivers and outfitted with commonly used hardened peripherals, the Zynq-7000S delivers cost-optimized system integration ideal for industrial IoT applications such as motor control and embedded vision.



Zynq Z-7000S SoC Device Block Diagram

Zynq-7000

Zynq-7000 devices are equipped with dual-core ARM Cortex-A9 processors integrated with 28nm Artix-7 or Kintex®-7 based programmable logic for excellent performance-per-watt and maximum design flexibility. With up to 6.6M logic cells and offered with transceivers ranging from 6.25Gb/s to 12.5Gb/s, Zynq-7000 devices enable highly differentiated designs for a wide range of embedded applications including multi-camera driver’s assistance systems and 4K2K Ultra-HDTV.



Zynq Z-7000 SoC Device Block Diagram

Zynq®-7000 All Programmable SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory, AXI 64b ACP, 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	1.8Mb (50)	2.5Mb (72)	3.8Mb (107)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.1Mb (545)	26.5Mb (755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
	Speed Grades: Commercial	-1			-1			-1			-1
	Speed Grades: Extended	-2			-2,-3			-2,-3			-2
	Speed Grades: Industrial	-1, -2			-1, -2, -1L			-1, -2, -2L			-1, -2, -2L

Notes:
1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. See DS190, *Zynq-7000 All Programmable SoC Overview* for details.
2. Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* for more details.
3. Security block is shared by the Processing System and the Programmable Logic.

Zynq-7000 SoC Device Table

Mechanical Parameters

- Dimensions: 75mm x 50mm (10-layer PCB design)
- Power supply: 5V
- Working temp.: -40~85 Celsius (industrial grade)

SoC

- Xilinx XC7Z010-1CLG400I (Zynq-7010) / XC7Z020-2CLG400I (Zynq-7020) SoC
  - ARM® Cortex™-A9 MPCore processor
  667MHz dual-core processor (up to 866MHz, for XC7Z010 or XC7Z020)
  - Integrated Artix-7 class FPGA subsystem
  with 85K logic cells, 53,200 LUTs, 220DSP slices (for XC7Z020)
  with 28K logic cells, 17,600 LUTs, 80 DSP slices (for XC7Z010)
  - NEON™ & Single / Double Precision Floating Point for each processor
  - Supports a Variety of Static and Dynamic Memory Interfaces

Memory

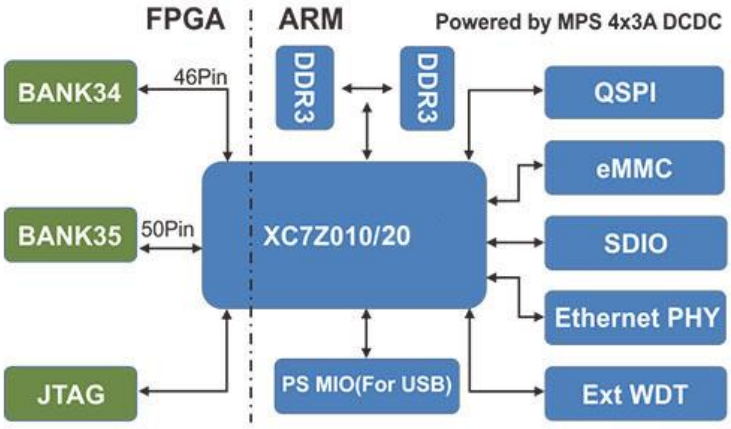
- 512MB DDR3 SDRAM (256MB*2）
- 4GB eMMC
- 16MB QSPI Flash

Peripherals and Signals Routed to Pins

- 10/100/1000M Ethernet PHY (YT8521SH)
- External watchdog
- Three LEDs
  - One red LED for power indicator
  - One green LED for FPGA program done indicator
  - One green user LED for system indicator
- 1.27mm pitch 180-pin Stamp Hole Expansion Interface brings out below signals:
  - One Gigabit Ethernet
  - One USB
  - Two Serial ports
  - Two I2C
  - Two CAN BUS
  - Two SPI

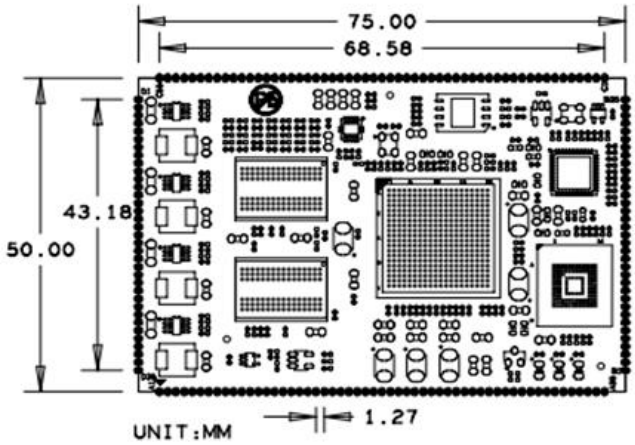
  * Serial ports, I2C, CAN and SPI signals in PS part can be implemented through PL pins via Emio.
  - Two ADC (16-channel ADC brought out through PL pins)
  - One SDIO

Function Block Diagram



MYC-Y7Z010/20-V2 Function Block Diagram

Dimension Chart



Dimensions of MYC-Y7Z010/20-V2

Software Features

The MYC-Y7Z010/20-V2 CPU Module is capable of running Linux 4.14. MYIR provides software package in product disk along with the goods delivery. The software package features as below:

Item	Features	Description	Remark
Cross compiler	gcc 6.2.1	gcc version 6.2.1 20161114 (Linaro GCC Snapshot 6.2-2016.11)	
Boot program	BOOT.BIN	First boot program including FSBL, bitstream	Source code provided
	u-boot	Secondary boot program	Source code provided
Linux Kernel	Linux 4.14	Customized kernel for MYD-Y7Z010/20-V2	Source code provided
Drivers	USB Host	USB Host driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	CAN	CAN driver	Source code provided
	LCD Controller	XYLON LCD driver	Source code provided
	HDMI	HDMI (SII902X chip) driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	QSPI	QSPI Flash W25Q128FW driver	Source code provided
	RTC	DS3231 RTC driver	Source code provided
	Resistive Touch	TSC2007 resistive touch screen driver	Source code provided
	Capacitive Touch	FT5X0X capacitive touch screen driver	Source code provided
	ADC	ADC driver	Source code provided
File System	Ramdisk	Ramdisk system image	
	Rootfs.tar	Tar file	

Linux Software Package Features

Order Information

Item	Part No.	Packing List
MYC-Y7Z010/20-V2 CPU Module	MYC-Y7Z010-V2-4E512D-667-I (for XC7Z010-1CLG400I)	✓ One MYC-Y7Z010-V2 CPU Module
	MYC-Y7Z020-V2-4E512D-766-I (for XC7Z020-2CLG400I)	✓ One MYC-Y7Z020-V2 CPU Module
MYD-Y7Z010/20-V2 Development Board	MYD-Y7Z010-V2-4E512D-667-I (for XC7Z010-1CLG400I)	✓ One MYD-Y7Z010/20-V2 Board ✓ One 1.5m cross Ethernet cable ✓ One DB9 converting cable ✓ One Power converting cable ✓ One 12V/1.25A Power adapter
	MYD-Y7Z020-V2-4E512D-766-I (for XC7Z020-2CLG400I)	

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